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ABSTRACT OF THE DISCLOSURE

2 A semiconductor apparatus including programmability that may allow a SSTL
3 interface or LVTTL interface is provided. A reference configuration circuit **(100)** may
4 provide a primary reference potential VREF0 and secondary reference potential VREF.
5 Reference configuration circuit **(100)** may include a bond pad **(PAD1)**, a reference potential
6 generation circuit **(1)**, a control circuit **(50)**, a reference selection circuit **(60)**, and a
7 secondary reference potential generation circuit **(70)**. During a wafer test mode, primary
8 reference potential VREF0 and secondary reference potential VREF may be provided from a
9 potential that may be applied to bond pad **(PAD1)**.